A METHOD TO SYNCHRONISE DATA AND A TRANSMITTER AND A RECEIVER REALISING SAID METHOD

The present invention relates to a method to synchronise data as described in the preamble of claim 1, and a transmitter and a receiver realising said method as described in the preambles of claim 4 and claim 6.

Such a method to synchronise data is common knownledge. Indeed, e.g. in communication systems where data is sent from a transmitter to a receiver, for the receiver to be able to interprete the received data, the received data have to be synchronised in the receiver with a reference signal, usual a clock signal of the receiver. Realising synchronisation implies more complexity and therefore there is a need for additional hardware or software in the receiver. The trade-offs are generally between expense and complexity, on one hand, and error performance on the other hand. However, some kind of receivers e.g. receivers using asymmetric digital subscriber line technology are required to have both, a low complexity and also a low error performance.

An object of the present invention is to provide a method to synchronise data and a transmitter and a receiver realising said method of the above known type but which are suited for use in communication systems where a low complexity and a low error performance are required at the receiving side of the communication system.

According to the invention, this object is achieved by the method to synchronise data as described in claim 1, and the transmitter and the receiver realising the method as described in claim 4 and claim 6, respectively.

Indeed, due to the trigger signals generated from the signal available in the receiver and sent to the transmitter, the transmitter is able to send the data to the receiver upon receipt of the trigger signals i.e. at the right time to ensure synchronisation between the data received in the receiver and the available signal e.g. a clock signal in the receiver. In this way, the complexity of the synchronisation process is moved from the receiver side to the transmitter side of the communication system and each level of synchronisation can be realised with

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the required level of error performance and without making the receiver too complex.

Another characteristic feature of the present invention is that the data, sent from the transmitter to the receiver, is asynchronous data. Indeed, upon receipt of the trigger signals, the transmitter must be able to send data even if the trigger signals are sent in an asynchronous way. This is for instance the case when the receiver has to receive the data at a time moment at which the data has just to fit at a predefined place in a frame. In this way frame synchronisation is achieved.

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Yet another characteristic feature of the present invention is that in the event that no data is available in the transmitter to be sent upon receipt of the trigger signals, the transmitter is able to generate idle data and to send this idle data to the receiver. In this way, e.g. the frame synchronisation proces is not disturbed. This is described in the method of claim 3 and the transmitter of claim 8.

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An important application of the present invention is that the receiver is included in an asymmetric digital subscriber line (ADSL) modem. This is described in claim 5. In such receiver, the received data is framed into an asymmetric digital subscriber line frame and sent over twisted pair. However in known ADSL modems using the known synchronisation methods, when the modem receives data at a higher frequency than the frequency at which the data is sent, the data has to be buffered before being framed. As already mentioned above, it is important to keep the complexity of a receiver in such a modem low. By using the method of the invention, the asymetric digital subscriber line modem gets rid of the buffering aspect. In fact the buffering is again moved from the receiver to the transmitter which now must be able to buffer the data until he receives a trigger signal of the receiver to have the permission to sent the data to the receiver. Therefore, this way of synchronising is expecially suited for systems wherein there is anyway buffering foreseen at the transmitting side, e.g. for Asynchronous Transmission Mode (ATM) systems.

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The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying figure which is a block scheme of a synchronisation system including a transmitter and a receiver realising the method of the invention.

Referring to the figure, the working of the synchronisation system will be described. First, the working of the synchronisation system will be explained by means of a functional description of the blocks shown in the Figure. Based on this description implementation of the functional blocks will be obvious to a person skilled in the art and will therefor not be described in detail. In addition, the principle working of the synchronisation system will be described in further detail.

The synchronisation system includes a transmitter TX and an asymmetric digital subscriber line modem (ADSL modem) ADSL.

The transmitter TX includes four functional blocks :

- a buffer BUF;
- an idle data generating means ID-GEN ;
- a data sending means DAT-SEND; and
- a trigger receiving means T-RX.

The buffer BUF is included to buffer the data DAT presented to the transmitter TX. This data DAT can be digital data of any kind, however, for this embodiment the data DAT is asynchronous data i.e. data organised following the asynchronous transfer mode (ATM) technique. As mentioned, the buffer BUF buffers the data DAT presented to the transmitter TX. However, it has to be understood that the buffer BUF will only do this when it is nessary i.e. when the transmitter receives more data DATA then he is allowed to send.

The idle data generating means ID-GEN is included to generate idle data. It has to be remarked that this one of the typical ATM functionalities. Idle data is send whenever there is no information available at the side of the sender at the moment of transmission. They allow a full asynchronous operation of both sender and receiver.

The data sending means DAT-SEND is included to send data from the transmitter TX to the ADSL modem. This data can be useful user information i.e. the data DAT coming from the buffer BUF or idle data, coming from the idle data generating means ID-GEN.

The trigger receiving means T-RX is included to receive trigger signals T coming from the ADSL modem. Upon receipt of such a trigger signal, the data sending means DAT-SEND is on his turn triggered by the trigger receiving means T-RX and is allowed to send data.

The ADSL modem includes besides a receiver RX also the characteristic functional blocks of an ADSL modem. Since the description of the ADSL technology goes beyond the scope of this invention, these functional blocks are not shown in the figure. However, it is worth to mention here that one of the functional blocks of such an ADSL modem is a framer which organizes overhead information and user information i.e. the incoming data DAT into ADSL frames, i.e. uniformly sized groups of bits used to organize the ADSL data stream.

The receiver RX includes three functional blocks :

- trigger generating means T-GEN;
- trigger sending means T-SEND; and
- data receiving means DAT-RX.

The trigger generating means T-GEN is included to generate trigger signals T from an available signal SIG in the receiver RX. This available signal SIG is generated in accordance with the time moments whenever data DAT is needed to fit into an available ADSL frame on a predetermined place. This signal S is not necessary a clock signal. Indeed, looking to the form of an ADSL frame, not the whole frame must be filled with data DAT, so by consequence, the signal S is not a signal with a constant frequency.

It has to be remarked here that the trigger signals T are allowed to be of any kind e.g. one single bit pulse or a predefined codeword as long as the trigger generating means T-GEN of the receiver RX and the trigger receiving means T-RX of the transmitter TX are lined up with each other.

The trigger sending means T-SEND is included to send the trigger signals T from the receiver RX to the transmitter TX and the data receiving means DAT-RX is included to receive the data DAT coming from the transmitter TX.

The transmission medium for sending the trigger signals is in the figure depicted as a separate line to simplify the description of the working of the system. However these signals can (and usually are) transmitted over the same transmission medium, i.e. twisted pair, as the data.

The principle working of the synchronisation system will be described in the following paragraph.

Whenever data DAT is needed to fit in an available ADSL frame on a predetermined place, a trigger signal T is generated from the available signal SIG and transmitted to the transmitter TX. Upon receipt of a trigger signal T the trigger receiving means T-RX gives a signal to the data sending means DAT-SEND, e.g. by means of a controle signal, and DAT-SEND on his turn requests data DAT to the buffer BUF. When there is data DAT available in the buffer BUF, the data DAT is provided to the data sending means DAT-SEND. However, when no data DAT is available in the buffer, the synchronisation process may not be disturbed and the data sending means DAT-SEND requests idle data to the idle data generating means ID-GEN. The data, either user data or idle data, is sent to the receiver RX and arrives there at the right moment to fit immediately into the ADSL frame on the predetermined place whereby synchronisation is established between the data DAT and the available signal SIG.

It has to be remarked that upon receipt of a trigger signal T, the transmitter TX has to send data DAT to the receiver RX. Sending data can be done immeditely after receiving of the trigger signal T, however the invention is not restricted to such kind of synchronisation systems but is also applicable for synchronisation systems where the data DAT is only sent after a predetermined period. Indeed, in this particular embodiment, the total period between the moment of generating a particular trigger and the moment of data DAT arriving at the receiver RX to fit into a according predefined ADSL frame must be taken into account at initialisation time. It can be necessary to have a predetermined

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waiting period somewhere in the loop in order to be able to realise the synchronisation. Since the complexity is moved from the receiver RX to the transmitter TX, this waiting period will also be realised by the transmitter TX.

It has to be remarked that due to the cell structure of the ATM data stream whenever idle data, not corresponding to a complete idle cell has been sent, that upon receipt of subsequent trigger signals T idle data has to be sent until the complete idle cell is transmitted, even if in the mean time some data DAT becomes available in the buffer BUF.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.